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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,624	06/30/2000	Stephen Jourdan	2207/8609	9451

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/608,624	JOURDAN ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-7,9-15,17-19 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-7,9-15,17-19 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 4-7, 19-15, 17-19 and 27 are rejected under 35 U.S.C. 102(a) as being anticipated by Jourdan et al. (eXtended Block Cache) herein referred to as Jourdan.

3. Regarding claim 4, Jourdan teaches a front-end system for a processor, comprising: an instruction cache system (see page 1, section 1); an extended block cache system (see page 3, section 3.1), comprising: a fill unit coupled to the instruction cache system (XFU, see page 3, right col. line 7), a block cache (Cache, see page 3, right col. line 5), a block predictor (XBTB, see page 3, right col. line 6), to store masks associated with complex blocks, the masks distinguishing block prefixes from each other (see page 6, first 10 lines); and a selector coupled to the output of the instruction cache system and to an output of the block cache (see page 6, Figure 5).

4. Regarding claim 5, Jourdan further discloses the block predictor coupled to the fill unit and the block cache (see page 6, Figure 5).

5. Regarding claim 6, Jourdan further discloses the block cache is to store blocks having a multiple-entry, single exit architecture (see page 5, right col., first paragraph).

6. Regarding claim 7, Jourdan further discloses the block predictor coupled to the fill unit and the block cache (see page 6, Figure 5).

7. Regarding claim 9, Jourdan discloses a method of managing extended blocks, comprising: predicting an address of a terminal instruction of an extended block to be used (by the XBTB; see page 6, left column, first 15 lines), determining whether the predicted address matches an address of a terminal instruction of a previously created extended block, and selecting one of the extended block in the event of a match (see page 5, section 3.5).

8. Regarding claim 10, Jourdan further discloses creating a new extended block when there is no match (see page 5, section 3.5, last 10 lines).

9. Regarding claim 11, Jourdan further discloses receiving new instructions until a terminal condition occurs, assembling the new instructions into an extended block, determining whether an address of a terminal instruction in the new block matches an address of a terminal instruction of a pre-existing block, and unless a match occurs, storing the new block in a memory (see section 3.3).

10. Regarding claim 12, Jourdan further discloses when an older block causes a match, storing the new block over the old block in a memory if the old block is subsumed within the new block(see page 5, left col.).

11. Regarding claim 13, Jourdan further discloses the storing comprises, when an older block causes a match, dropping the new block if the new block is subsumed within the older block (see page 5, left col.).

12. Regarding claim 14, Jourdan further discloses the storing comprises, when an older block causes a match, creating a complex block if the new block and the older block share a common suffix but include different prefixes (see page 5, left col.).

13. Regarding claim 15, Jourdan further discloses further comprising outputting instructions of the selected extended block for execution (see page 6, section 3.6).

14. Regarding claim 17, Jourdan discloses a processing engine, comprising: a front end stage storing blocks of instructions in a multiple-entry, single exit architecture when considered according to program flow (see page 5, right col. first diagram), and an execution unit in communication with the front end stage (see page 1, first diagram), wherein the front-end stage includes an instruction cache system, an extended block cache system (see page 6, section 3.6), including a fill unit provided in communication

with the instruction cache system (see page 6, Figure 4), a block cache (see fig. 3), and a selector coupled to the output of the instruction cache system and to an output of the block cache (see fig. 3).

15. Regarding claim 18, Jourdan further discloses the block cache is to store the multiple-entry, single exit traces (see abstract).

16. Claim 19 recites equivalent limitations as claim 5 and is rejected for the same reasons.

17. Regarding claim 27, Jourdan discloses a memory comprising storage for a plurality of traces (XBC, see page 5) and means for indexing the traces by an address of a last instruction therein according to program flow (by the XBTB; see page 6, left column, first 15 lines), wherein the traces include a plurality of instructions assembled according to program flow (see page 5, section 3.4) and at least one trace includes at least three segments of executable instructions in which, when considered according to program flow, first and second segments are mutually exclusive of each other and lead into the third segment (see page 5, first figure of right column).

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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